MOSFET AMPLIFIER

I shall chose one of the MOSFETs from the list of LTSpice library. It is **IRLML6346**, an International Rectifier device and the data sheet can be found here:

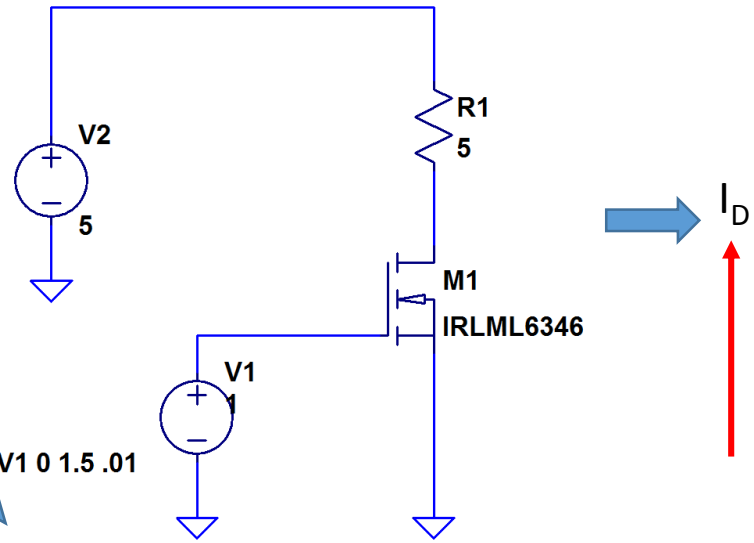
http://www.irf.com/product-info/datasheets/data/irlml6346pbf.pdf

Key features of the MOSFET : IRLML6346

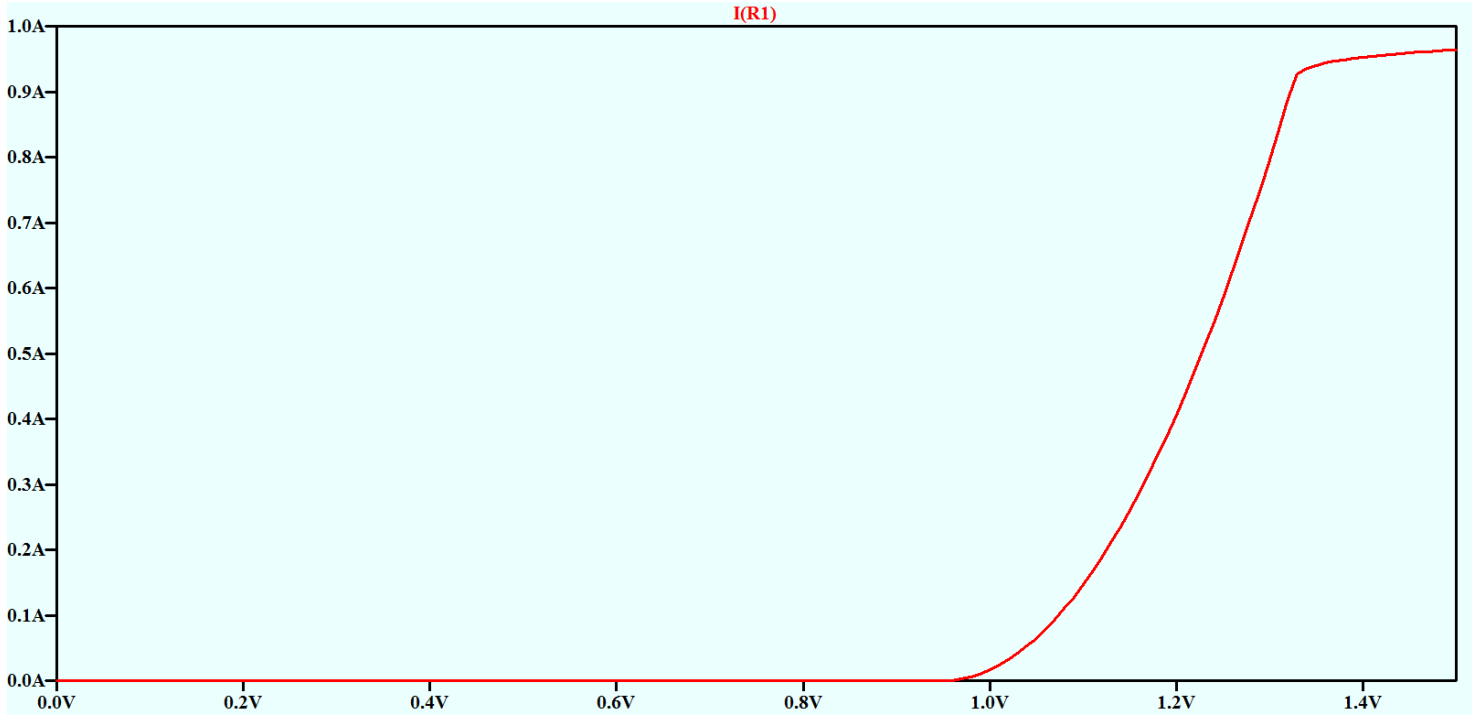
1. Maximum Drain-Source Voltage (V_{DS}): 30V
2. Gate Threshold Voltage $(V_{GS})_{(TH)}$: 0.5 – 1.1 V
3. Maximum Drain Current (I_D): 3.4 A
4. Maximum Power Dissipation (P_D): 1.3 W

Transconductance

Let us use LTSpice to find the transfer characteristics of the MOSFET. To do this the following schematic is drawn:

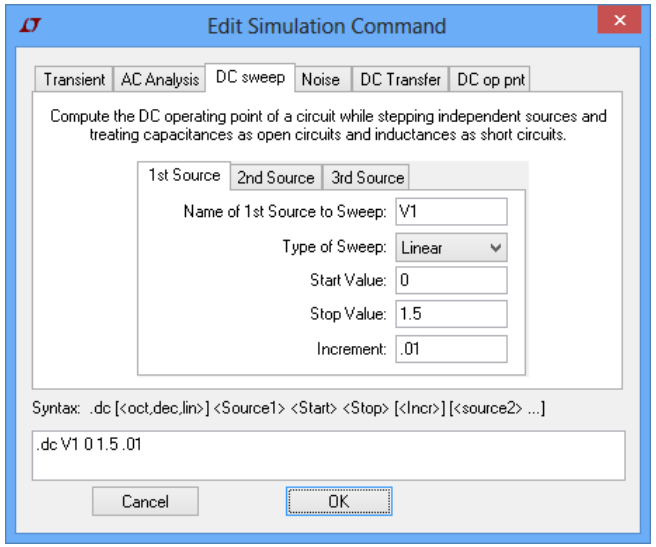


I_D



V_{GS}

In the EDIT SIMULATION window, we may use the Directive, which varies V1 fro 0 to 1.5V with step size 0.01V



Pressing RUN button gives us

From this graph we will find out the transfer characteristics, More commonly known as Transconductance: $\left(\frac{\Delta I_D}{\Delta V_{GS}}\right)$

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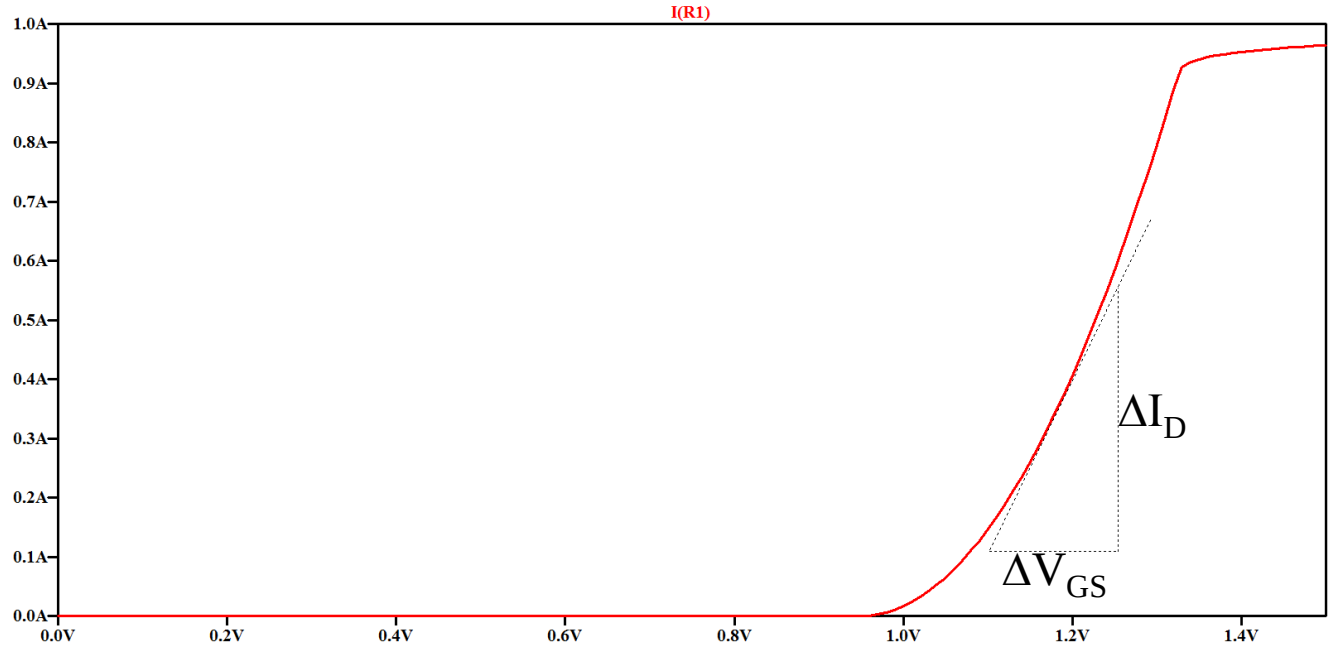
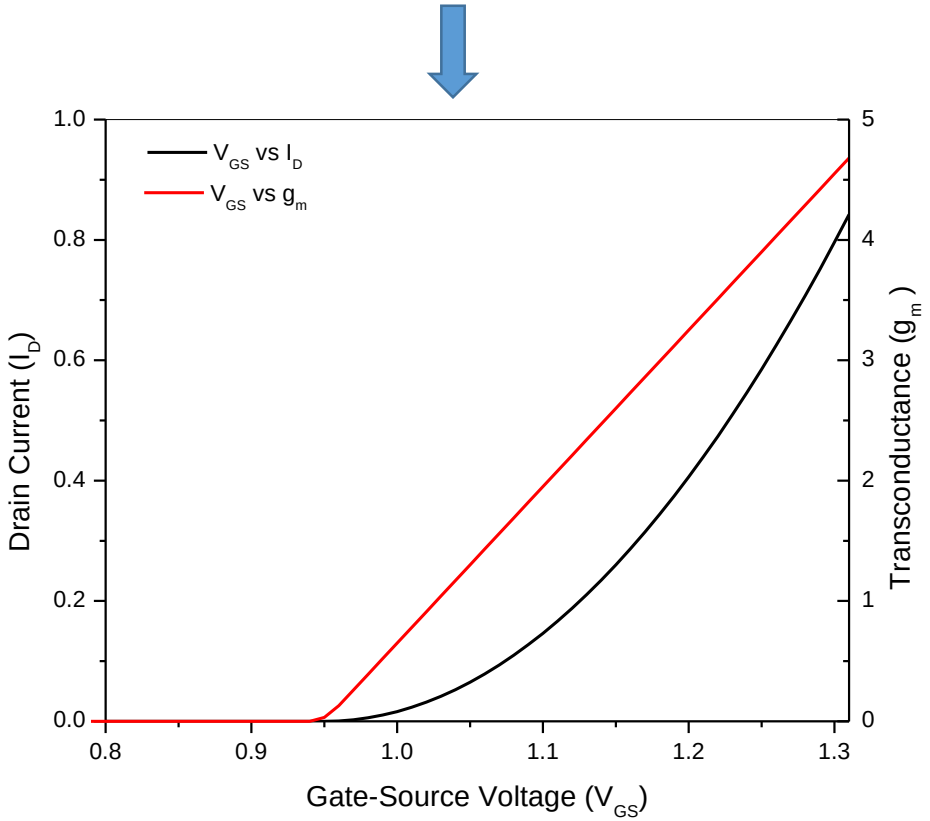
Transconductance

We can see that the transconductance, g_m varies as V_{GS} varies. The Higher the drain current, the higher is g_m



This can be more clearly shown below:



$$\text{Transconductance, } g_m = \left(\frac{\Delta I_D}{\Delta V_{GS}}\right)$$

$$I_D = K(V_{GS} - V_{TH})^2$$

$$g_m = \frac{d\,I_D}{d\,V_{GS}} = 2K(V_{GS} - V_{TH})$$

$$g_m = \frac{2\,I_D}{(V_{GS} - V_{TH})}$$

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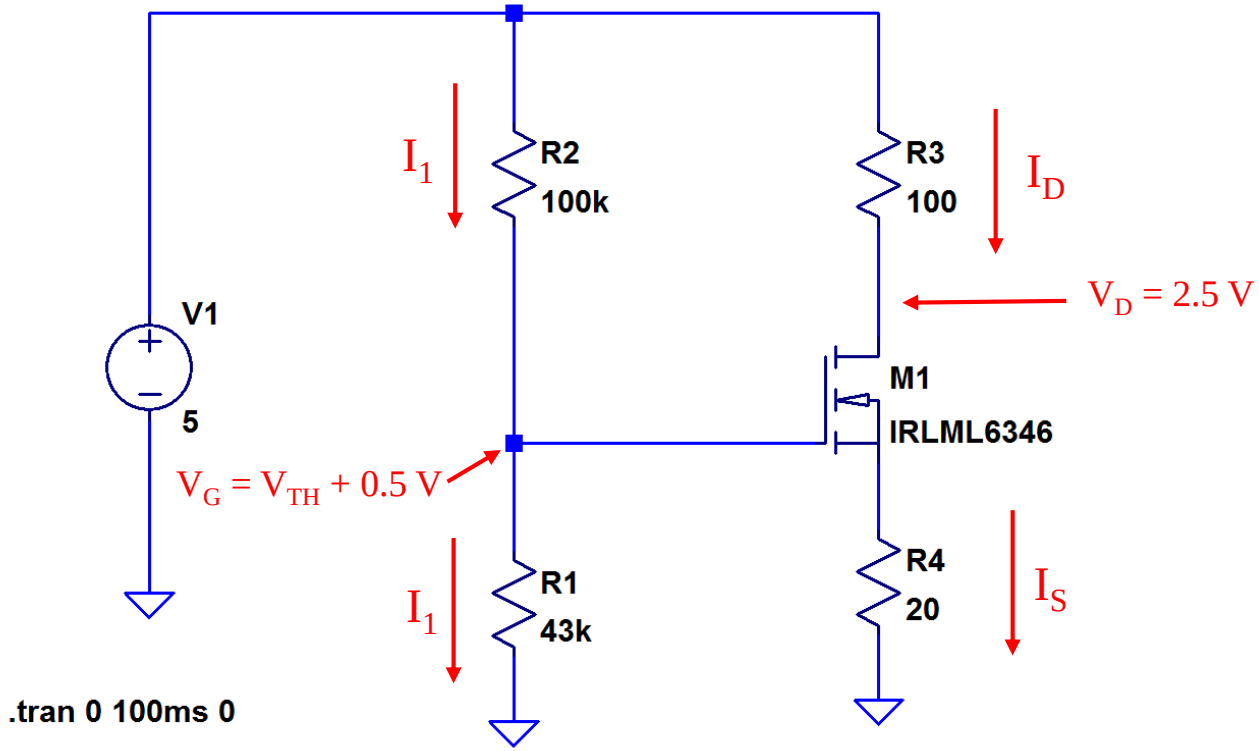
MOSFET Amplifier Biasing

Key Considerations:

1. Input impedance of MOSFET is very high, so R1 and R2 could be of high values (~ 100K)
2. R3 should be chosen considering the current and power handling capability of the MOSFET



Let us consider, we are using 5V supply voltage (V1). We are going to use this circuit diagram. First we have to choose the Value of R3. Let us consider V_D =2.5 V, to get the maximum output swing. So, voltage drop across R3 = V1-2.5 V = 2.5V. Current Id should be less than that can be handled by the MOSFET. Let us consider the value of R3=100 Ohm. So Id = 2.5/100 A = 0.025 A = 25 mA. Source current Is is equal to the drain current (25mA). For R4, less value will give us higher gain, at the expense of higher instability. Let us take this value, R4 = 20 Ohm. For Is = 25 mA, voltage drop (Vs) at R4 = 25 mAx20 = 0.5V. As MOSFET Gate acts like a capacitor, steady state gate current is zero, we can take the values of R2 and R1 several kilo Ohms, or hundreds of kilo Ohms. R1 and R2 are to be used as a voltage divider, with Vg to be equal to Vs +Vth. From the previous transconductance curve, we found Vth ~ 1V. So, Vg = 1+0.5 V = 1.5 V. If we take, R2 =100K, R1 becomes 42.85K, we may take 43K.

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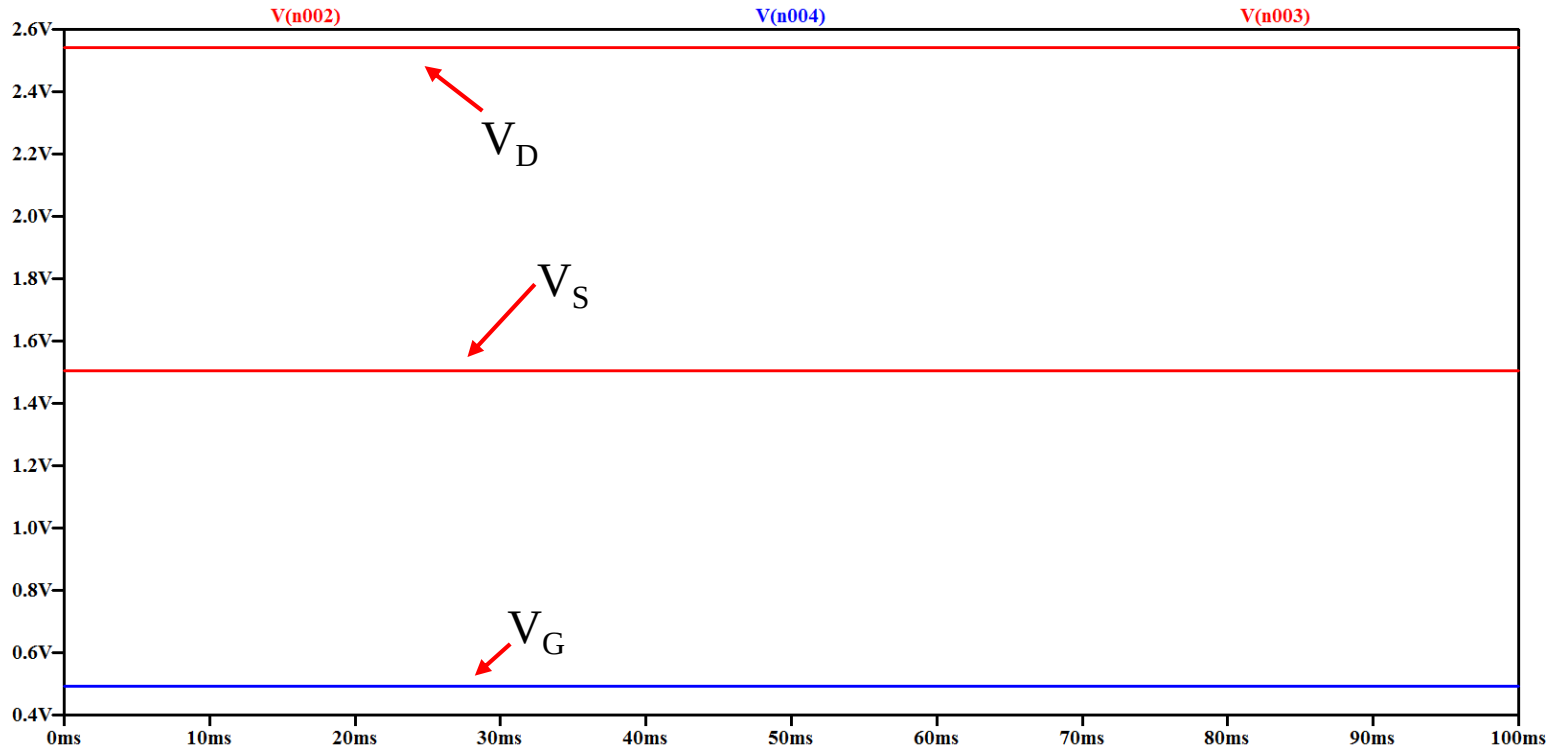
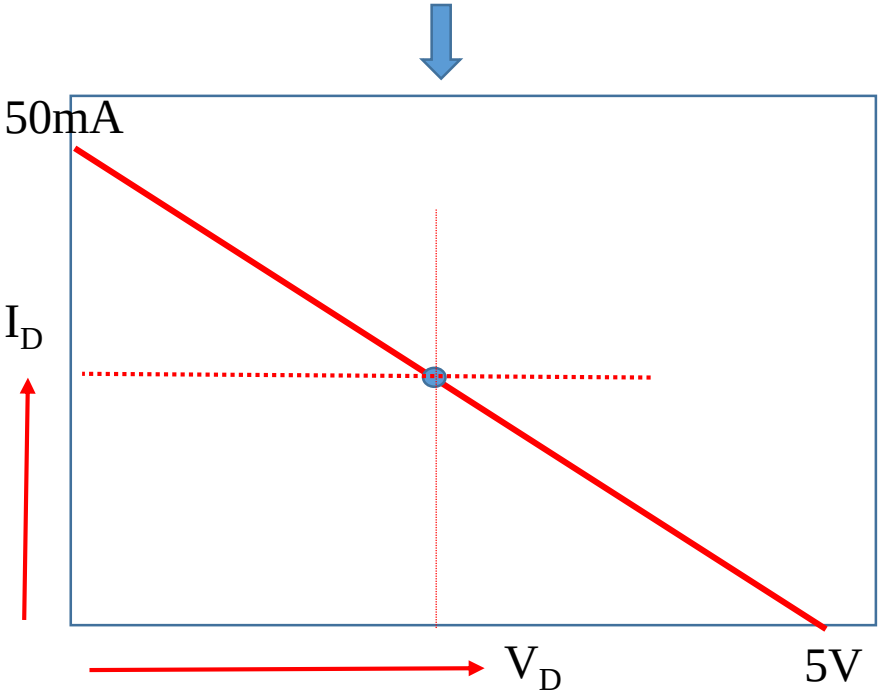
Simulated Results

The simulated results are shown, these closely matches that have been calculated. Simulation also shows the steady state power dissipation:~50mW.



The result can also be shown graphically using load line as shown



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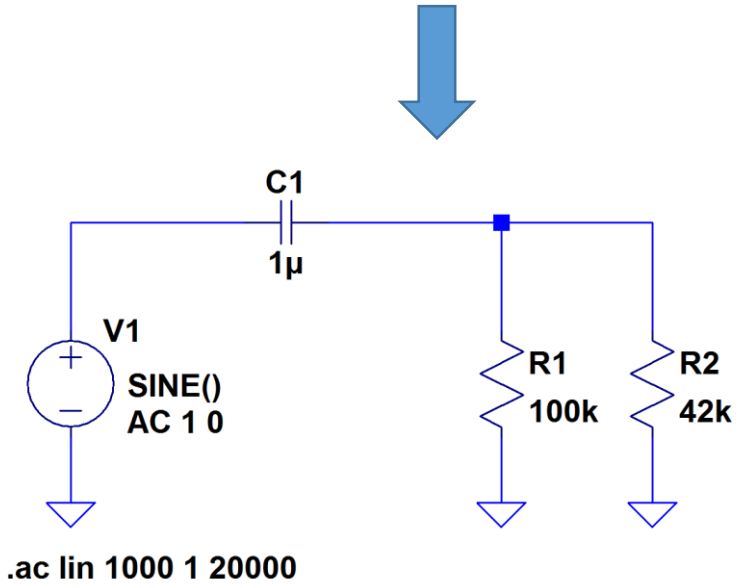
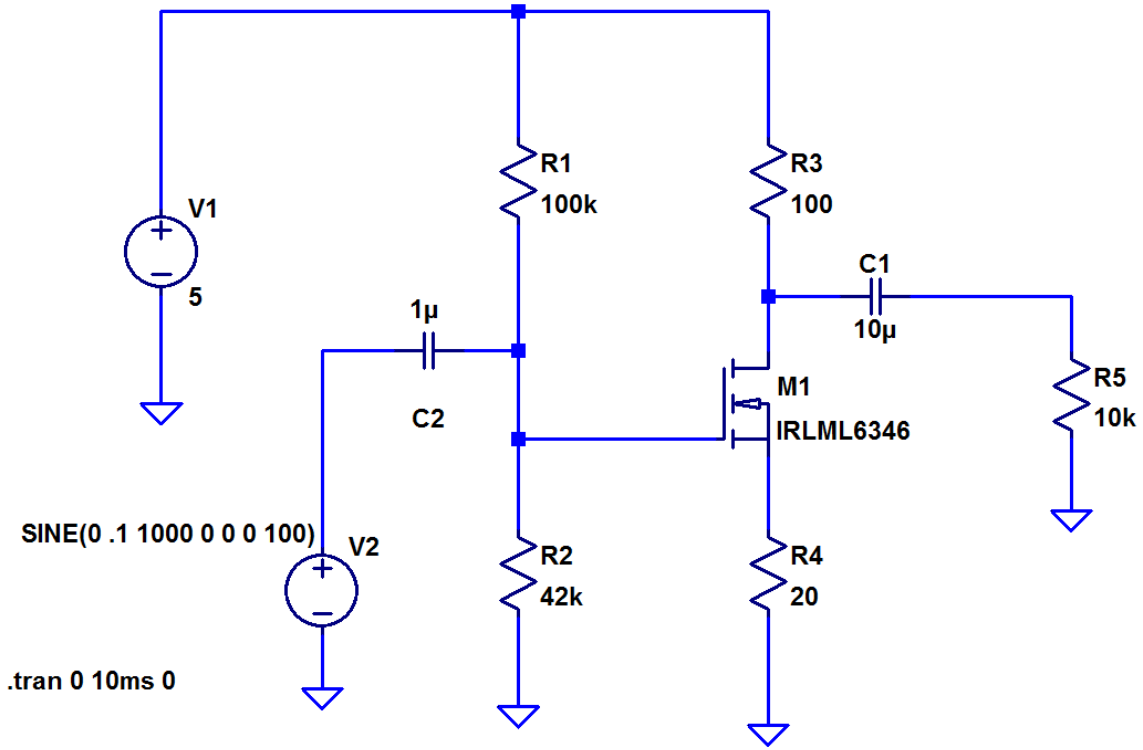
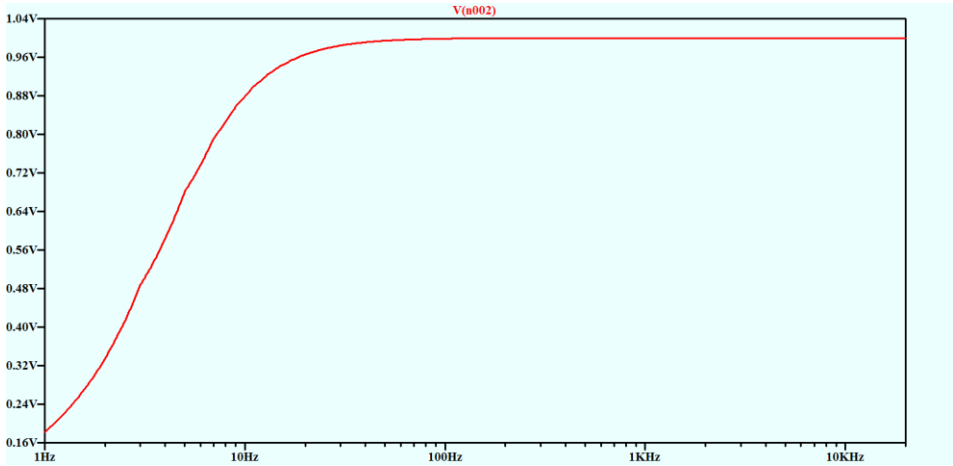
Amplifier: Input Coupling

After the biasing is done, then comes the matter of coupling AC signal to the amplifier and coupling a load at the output. For this we need two capacitors, one coupling signal to the Gate of the MOSFET, and the other at the Drain coupling the load as shown in the circuit. Let us first consider that the input signal is of low frequency like audio frequency (20 Hz – 20 kHz); for this range the MOSFET Gate capacitance won't affect. The input coupling circuit will look like:



AC simulation
Gives us this





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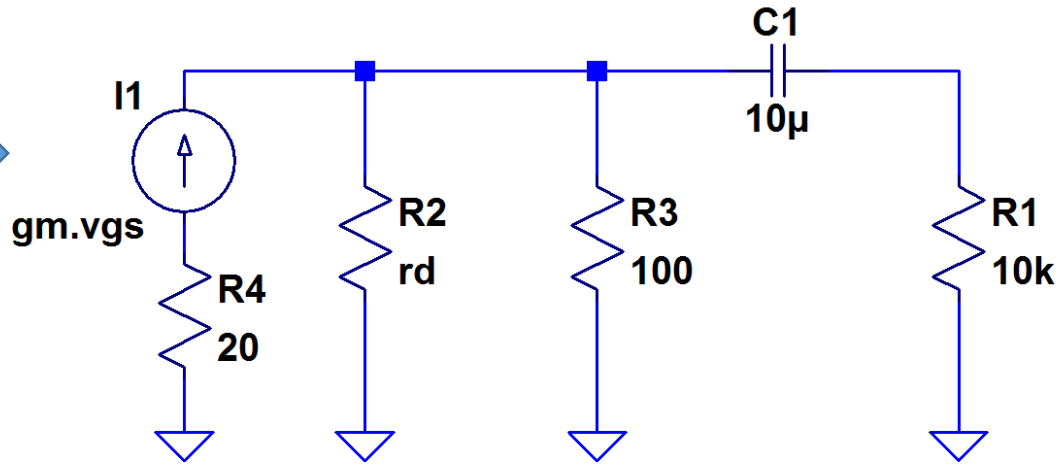
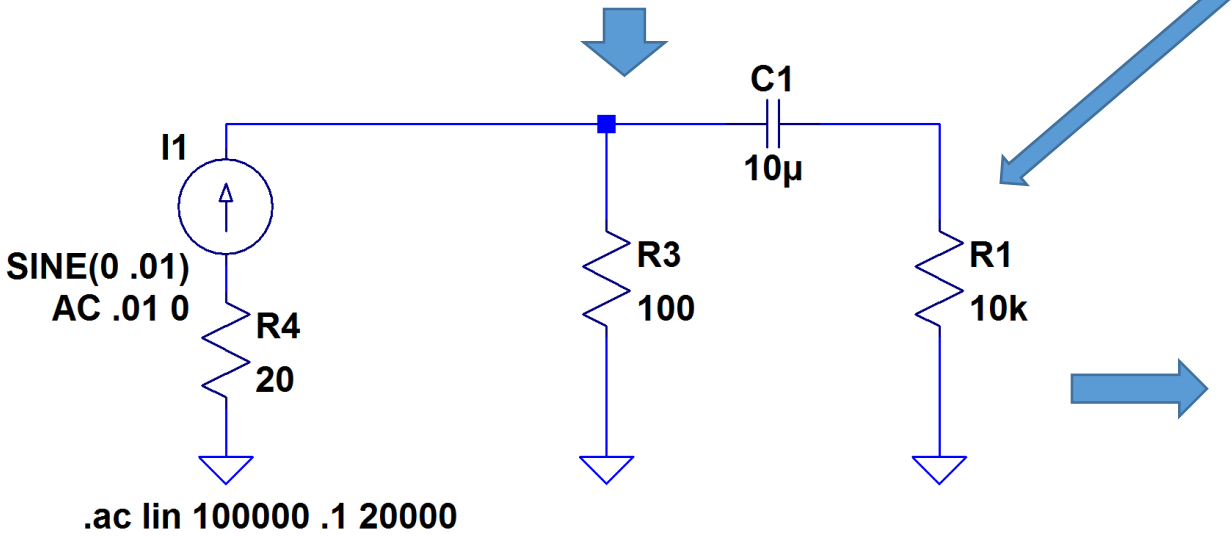
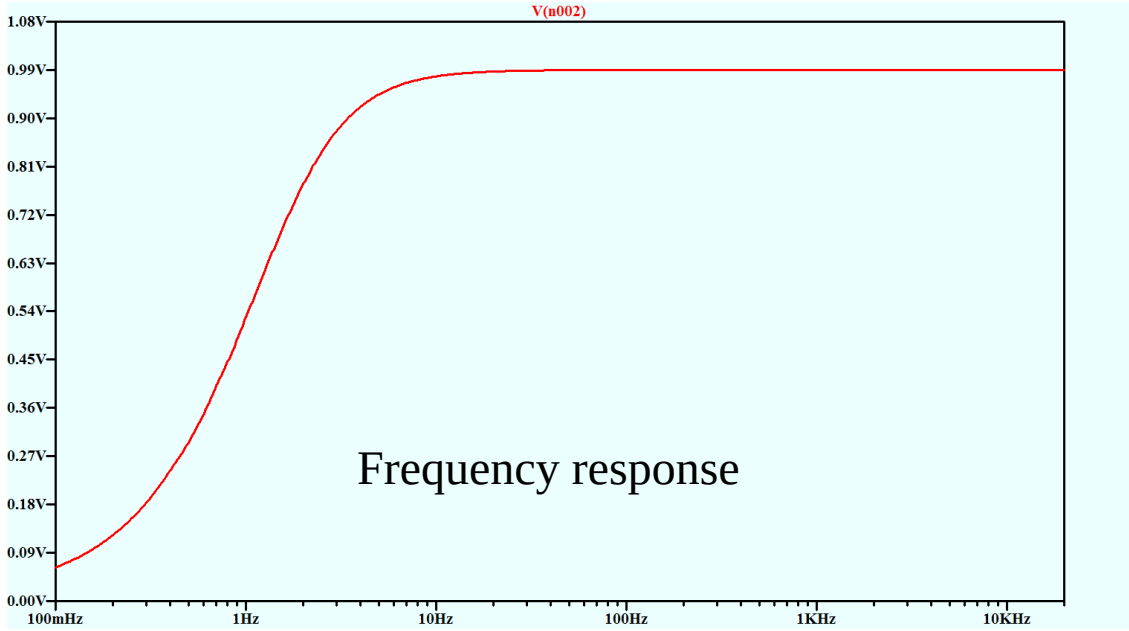
Amplifier: Output Coupling

Amplifier-output equivalent circuit can shown as



For LTSpice simulation we consider





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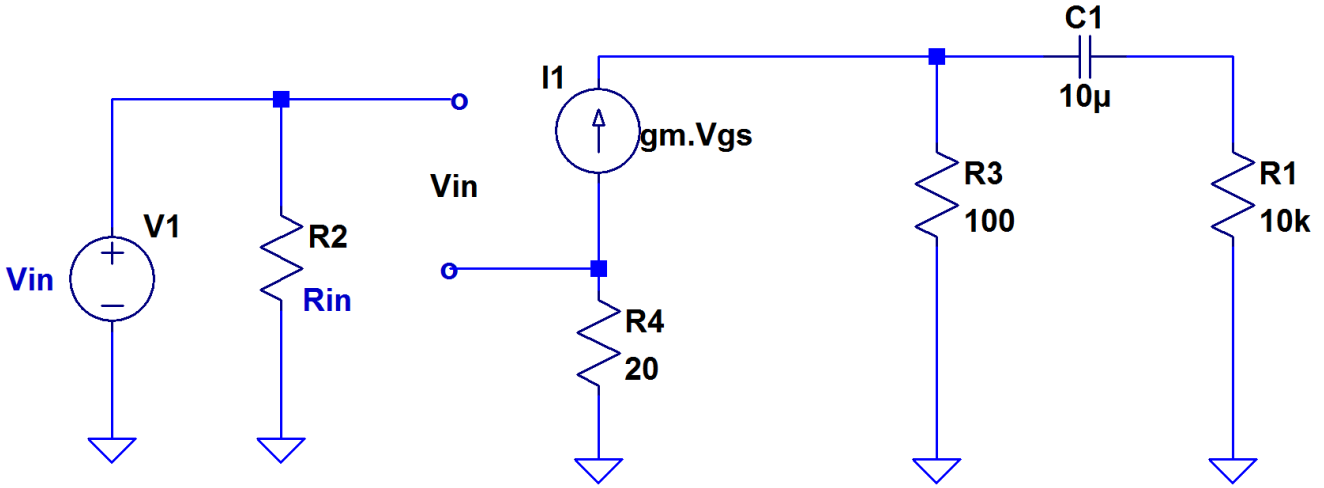
Amplifier - Gain

Small signal equivalent circuit is shown here

(v_o is the output and v_i is the input voltage)



$$V_o = g_m . v_{gs} . R_L$$

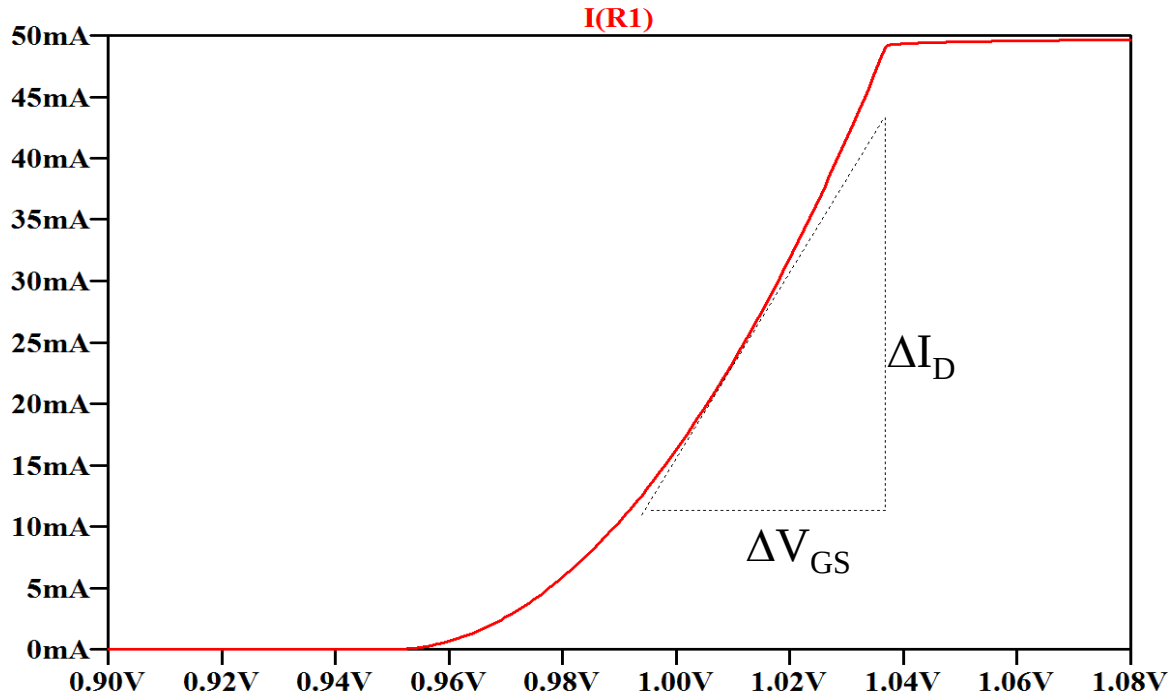
$$Where, R_L = R3 \,]]R1$$

$$V_i = v_{gs} + g_{m.}\, v_{gs} . R_4$$

Voltage gain A_v

$$A_v = \frac{v_o}{v_i} = \frac{g_m\, v_{gs}\, R_L}{v_{gs}\,(1 + g_m\, R_4)} = \frac{g_m\, R_L}{1 + g_m\, R_4}$$

We can find out the value of g_m at the biasing point (25 mA)
Using the transconductance curve



$$g_m = \Delta I_D / \Delta V_{GS} = 0.8\ A/V$$

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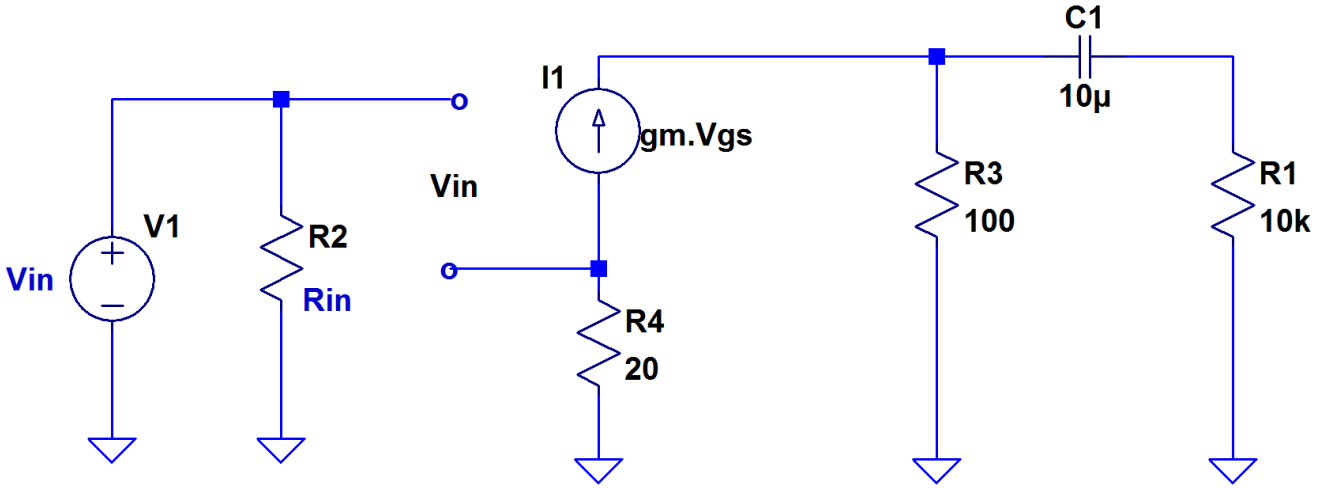
Amplifier - Gain

$$A_v = \frac{v_o}{v_i} = \frac{g_m R_L}{1 + g_m R_4}$$

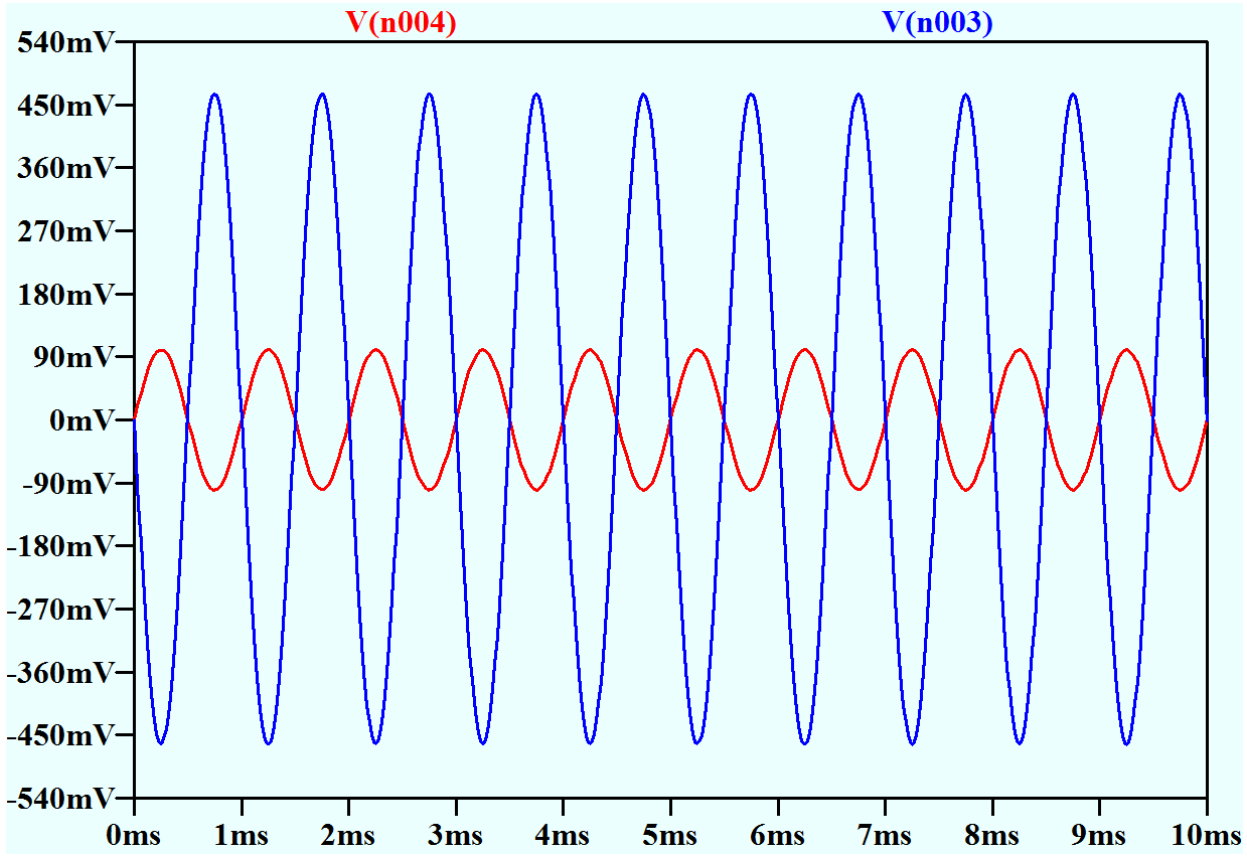
As the value of R1 is much higher than R3,
We may consider RL ~ R3

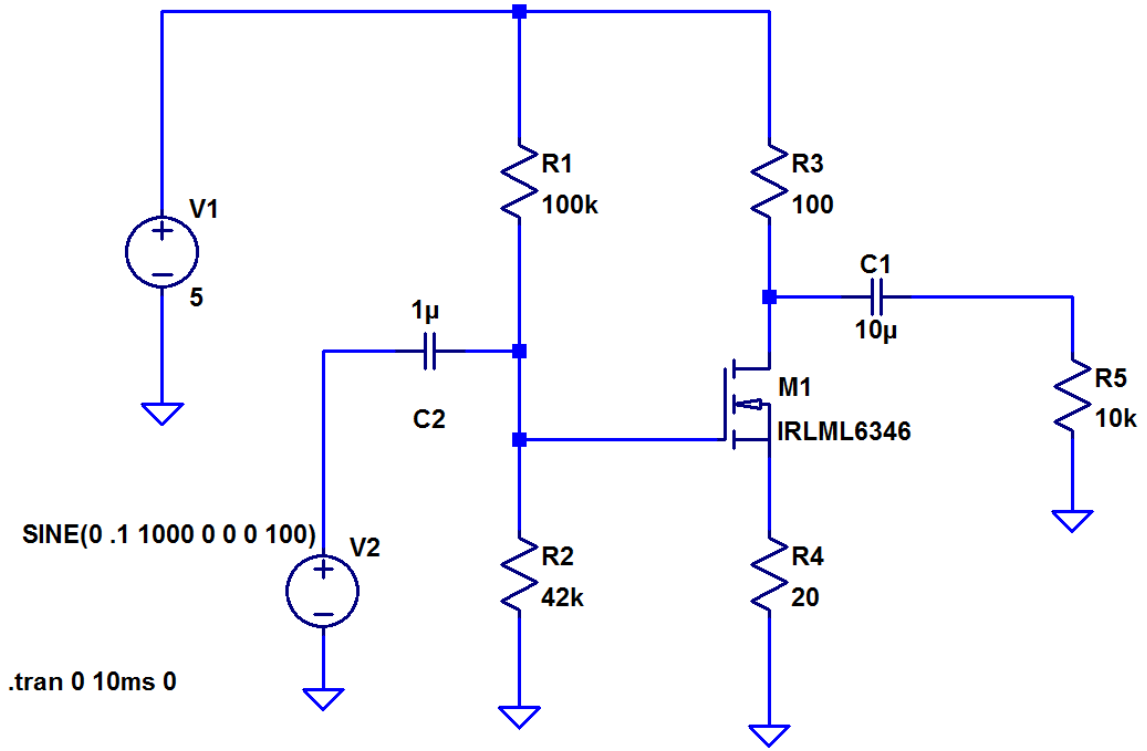


A_v = 0.8 x 100 / (1 + 0.8 x 20) = 4.7

Amplifier – Gain: Simulation Results

Simulation was run with input peak voltage 0f 100 mV and frequency of 1kHz. Simulation results are shown below, input being red and output being blue lines.





From these waveforms gain can be found:

$A_v = 472/102 = 4.63$

This is close to that of the calculated value

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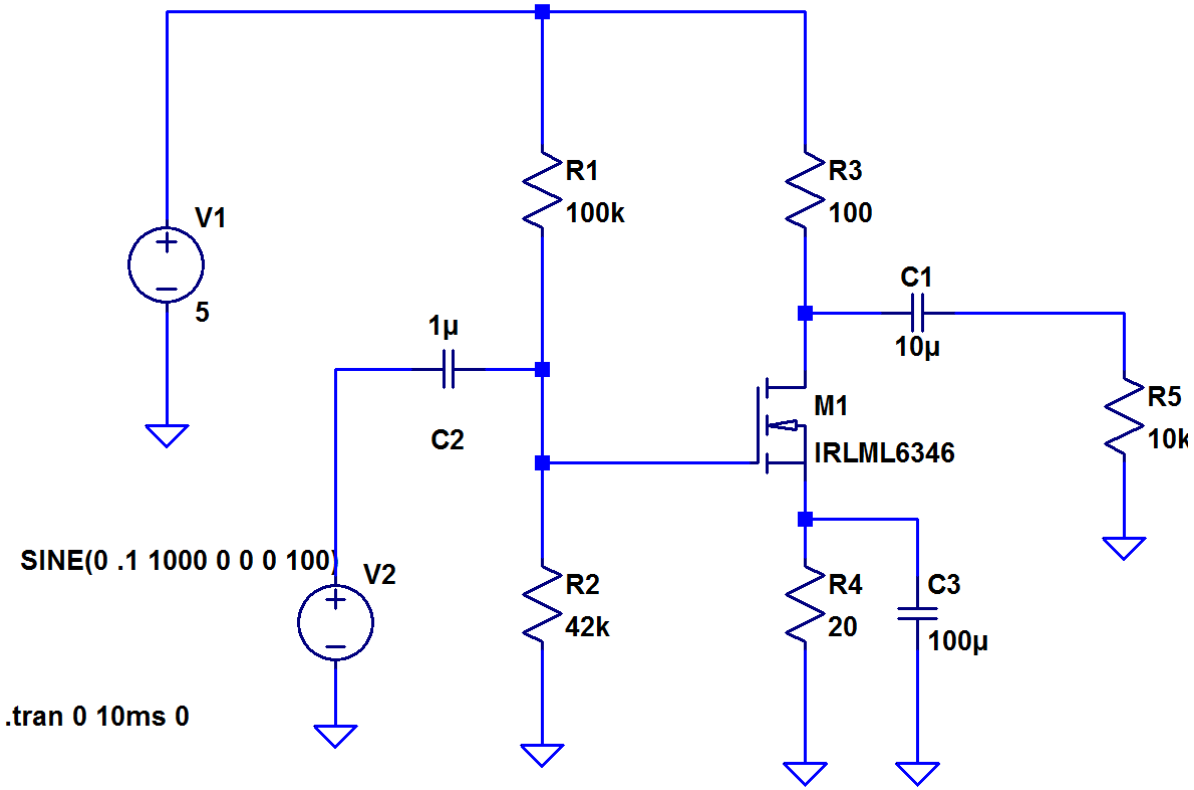
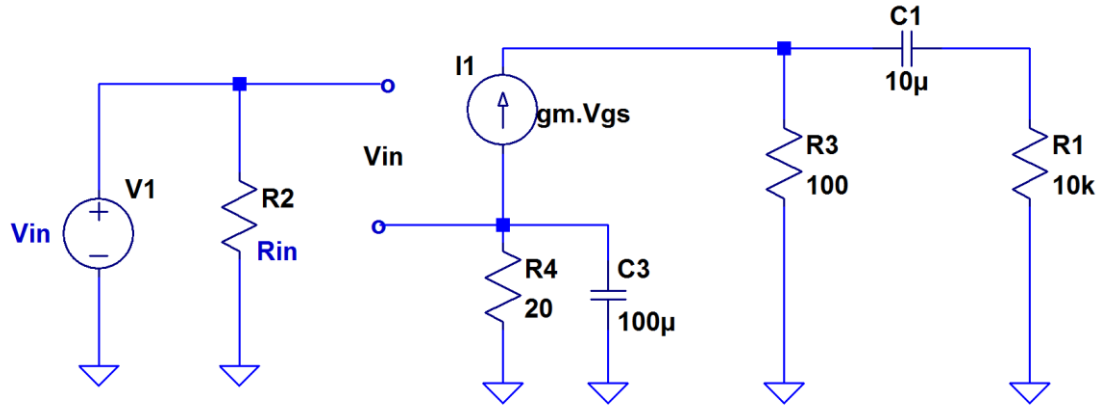
Gain Enhancement Using Source Bypass Capacitor





Equivalent circuit with bypass capacitor C3. At frequencies above tens of Hz, C3 nearly shorts the resistor R4 out.

Voltage gain becomes:

$$A_v = \frac{v_o}{v_i} = \frac{g_m R_L}{1 + g_m R_4} \approx g_m R_L = 0.8 \times 100 = 80$$

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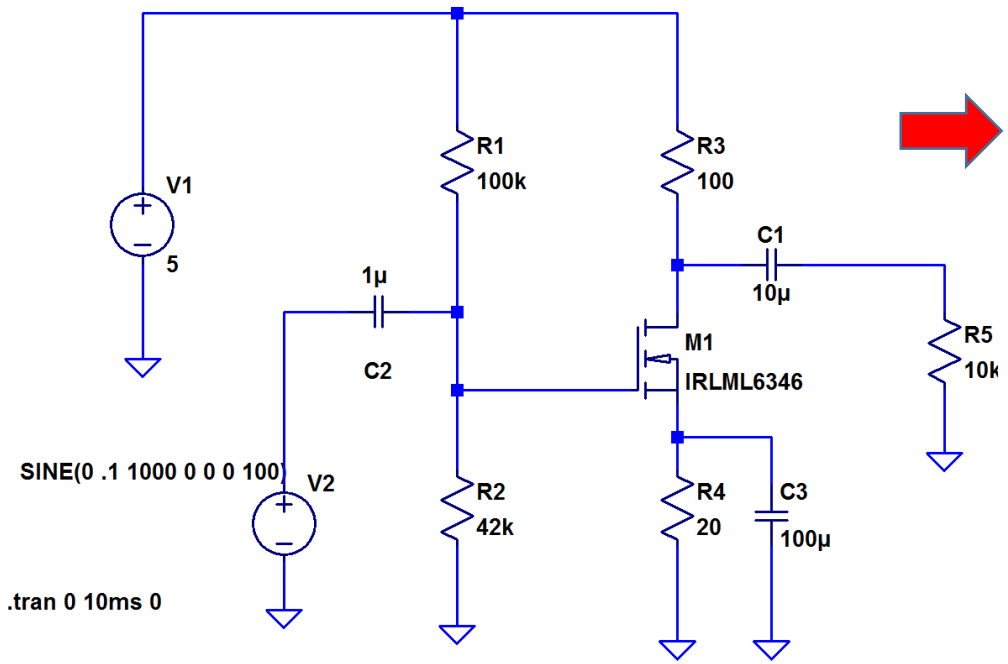
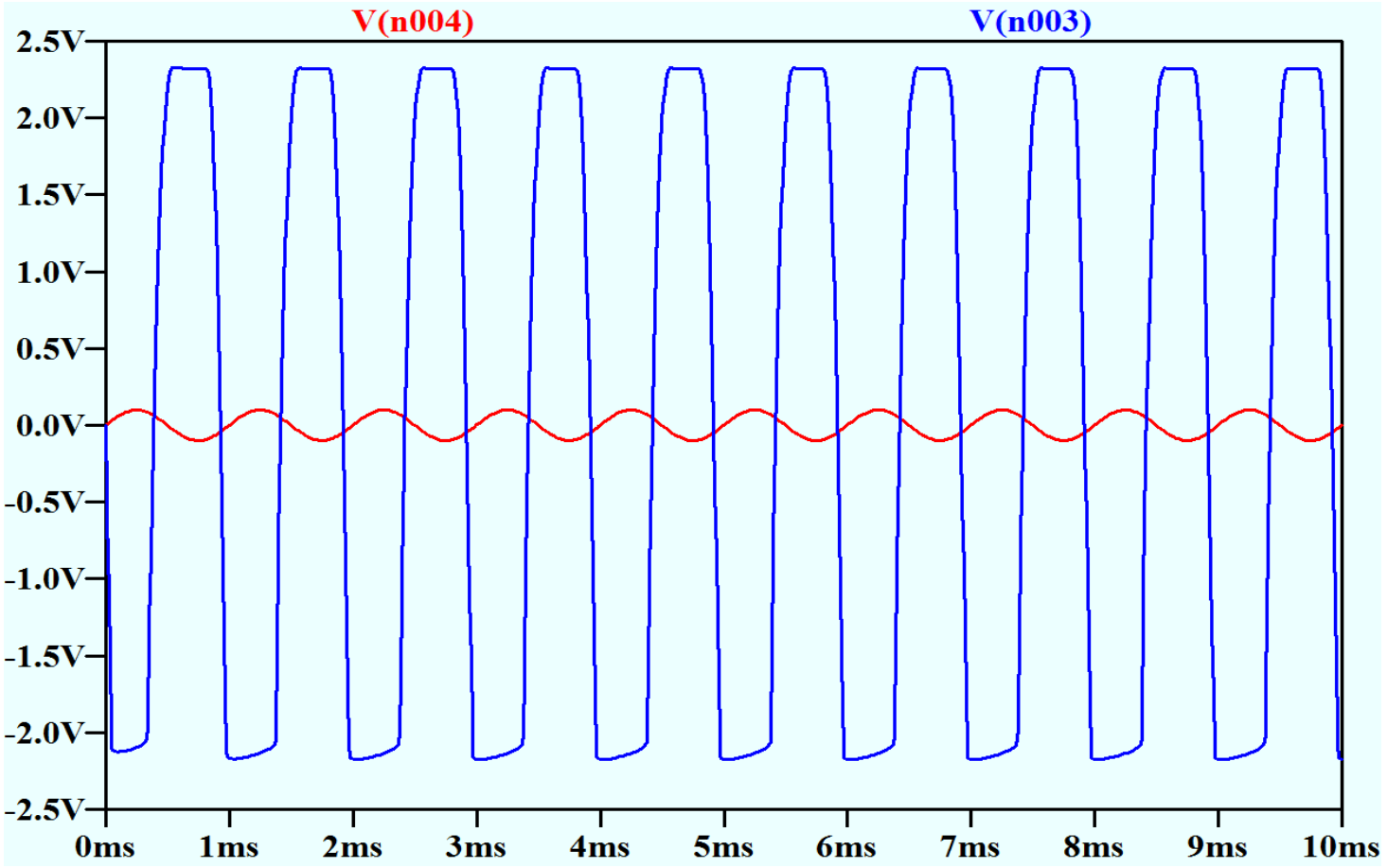
Simulation With Bypass Capacitor





As the voltage gain becomes 80, with the same input signal level (0.1V), the output is clipped as shown above. To get distortion less waveform we have to decrease the input level from 0.1 V to lower level.

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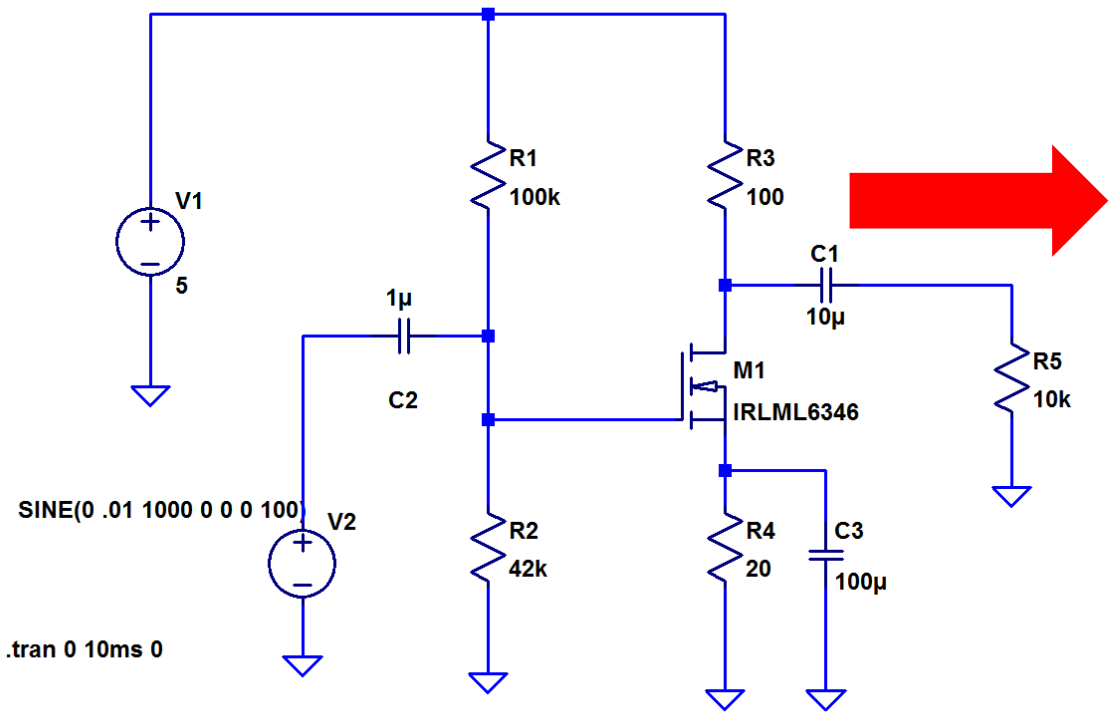
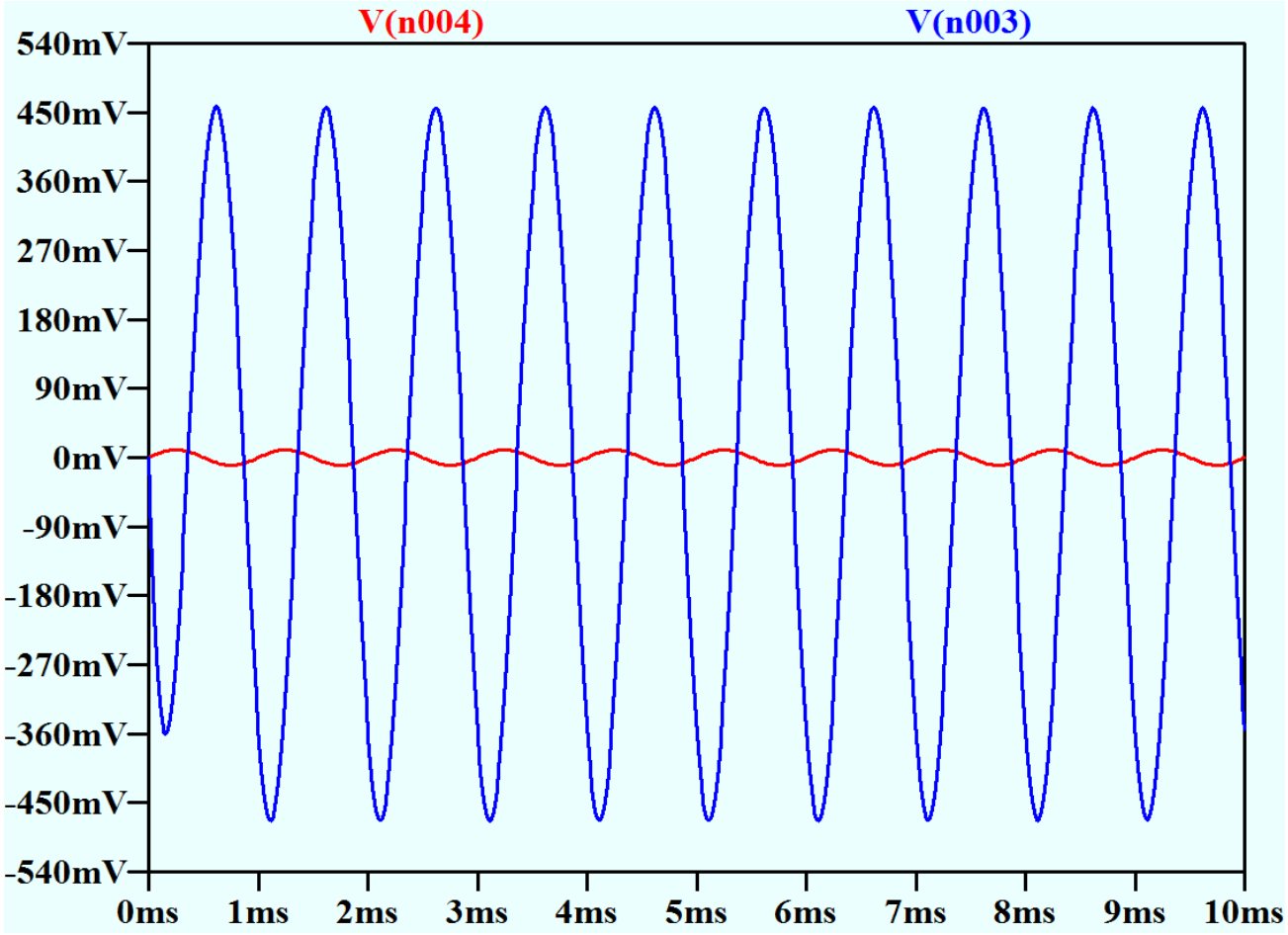
Simulation With Bypass Capacitor





Decreasing the input level to 0.01 V(10 mV), gives a good looking waveform at the output with a gain of 46. This discrepancy between the calculated value and the simulated value can be explained. We took input frequency 1kHz, at this frequency still the capacitive reactances (1/ ωc) are not sufficiently gone down. At 5kHz, the gain will reach 75, which can be easily simulated.

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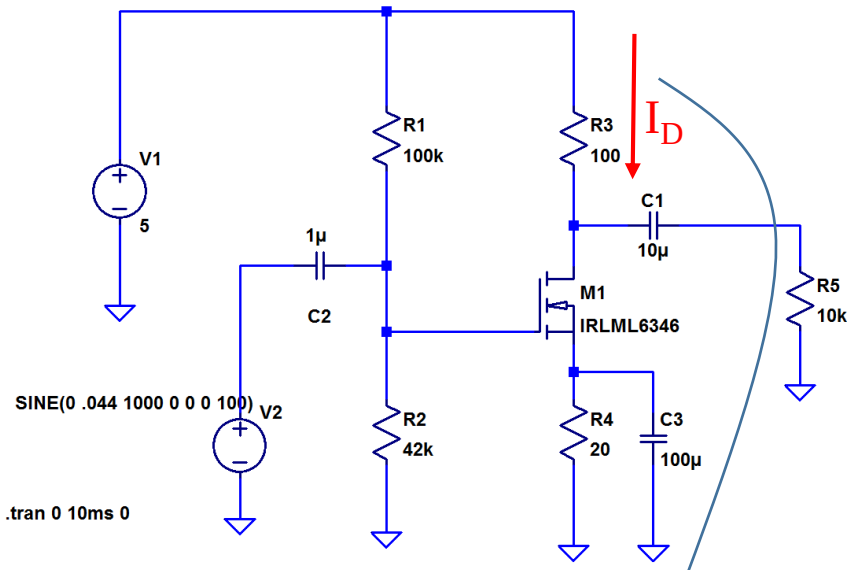
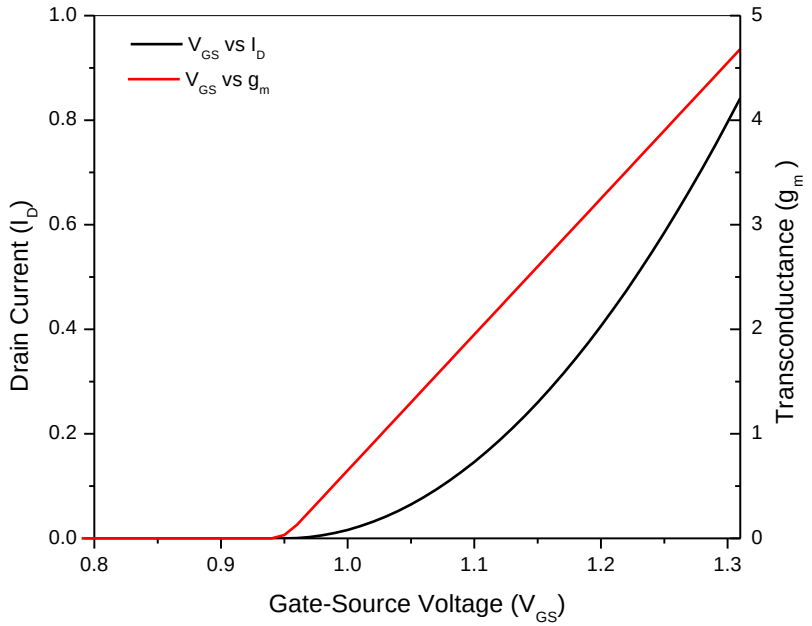
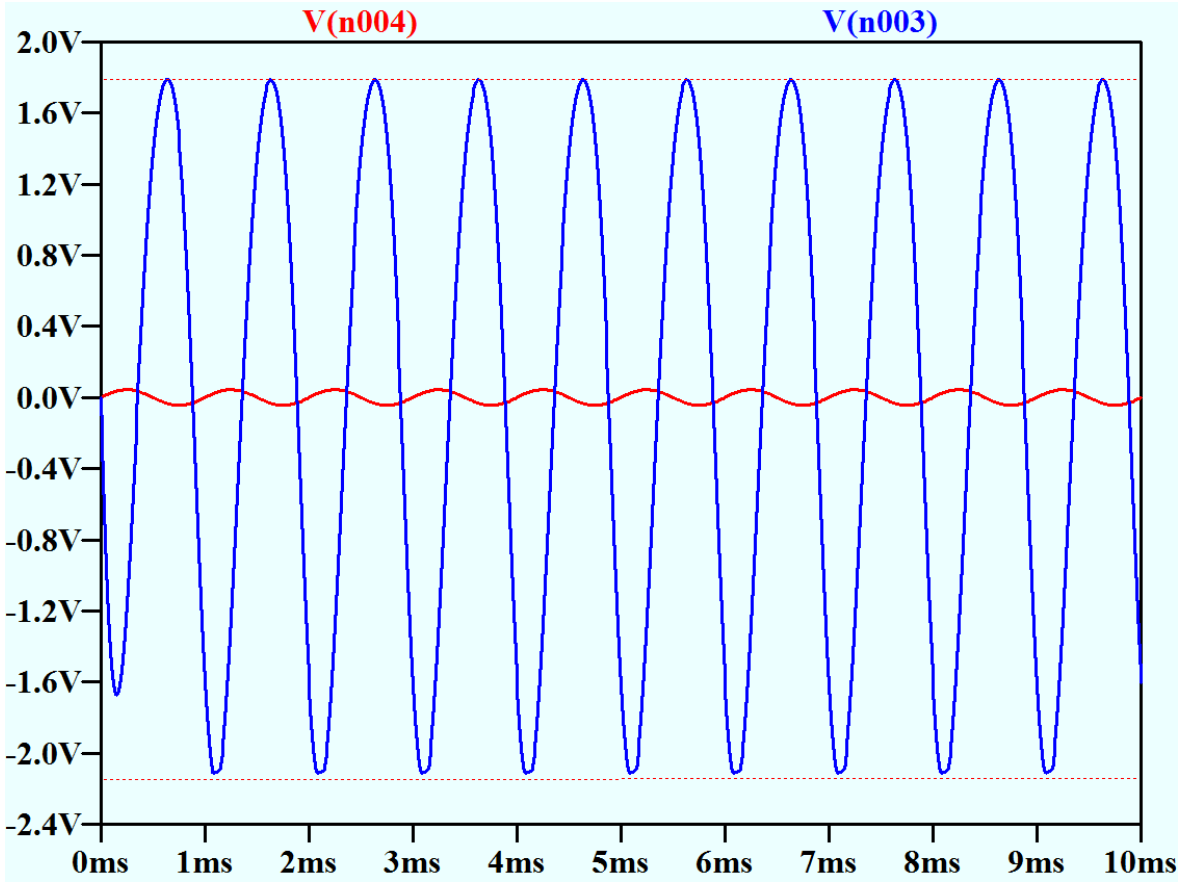
Simulation : Large Signal Input







If the input signal level is increased from 10 mV to ~ 45 mV, we get different amplification for positive and negative swing for the output signal. This is because at higher drain current transconductance goes higher

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